APPARATUS AND METHOD FOR AUTOMOTIVE BUS SWITCHING PROTECTION

Alexandre Pierre Palus

This application claims priority under 35 USC §119(e)(1) of Provisional Application Number 60/446,810 (TI-35999P) filed February 21, 2003.

1. Field of the Invention

This invention relates generally to data processing systems and, more particularly, to the transfer of signals between a central processing unit and associated peripheral units. The present invention is particularly relevant to automotive data processing systems.

2. Background of the Invention

For reasons of control and safety, data processing systems in automotive systems have become increasingly sophisticated. A central processing unit monitors sensors that measure parameters of the automotive unit operation. For example, the central processing unit can monitor signals identifying the rotation of the tires in the automotive unit and can provide control signals to relevant automotive components, for example in an anti-skid mode of operation. Similarly, sensors can provide the signals that result in the deployment of an air-bag. As consumers demand ever increasing capabilities, such as collision avoidance systems, the importance and complexity of the automotive data processing system can only increase.

Referring to Fig. 1, a typical system 10 for exchanging signals between a central processing unit 11 and a plurality of peripheral units, peripheral unit #1 121 through peripheral unit #N 12N. Each peripheral unit M 12M receives signals from the central processing unit via bus 14M and transmits signals to the central processing unit 11 via bus 15M.

By way of example, the peripheral unit could be a sensor system monitoring the rotation of a wheel. The

central processing unit sends initialization and time base signals to the sensor peripheral and receives signals indicative of the wheel rotation. The central processing unit can then process the signals according to a program.

In the automotive environment, the possibility of incorrect transmission of logic signals can potentially result in dangerous operation of the vehicle. In addition, because the length of conductors between a central processing unit and a peripheral unit is relatively long, the possibility of error generation in a transmitted signal is increased.

A need has therefore been felt for apparatus and an associated method having the feature that logic signals can be accurately transmitted in an automotive environment. It would be yet another feature of the apparatus and associated method to provide a signal indicating when a logic signal has been inaccurately transmitted. It would be a more particular feature of the apparatus and associated method to transmit both a logic signal and its complement to insure accurate transmission of the logic signal.

Summary of the Invention

The aforementioned and other features are accomplished, according to the present invention, by providing as part of a bus coupling a peripheral unit and the central processing unit, at least two associated conductors to transmitting a single signal. One of the associated conductors has a logic signal applied thereto. The associated conductor has complement logic signal applied thereto. At the output of the bus, the associated conductors are applied to a verification unit that verifies that the two associated conductors carry complementary logic signals. When the presence of complementary logic signals on the two associated conductors can not be verified, an exception condition is identified and appropriate response is taken by the data processing system.

Other features and advantages of the present invention will be more clearly understood upon reading of the following description and the accompanying drawings and claims.

Brief Description of the Drawings

Figure 1 is a block diagram of a data processing system having particular applicability to automotive data processing unit according to the prior art.

Figure 2 is a block diagram of technique for distribution of signals in an automotive data processing system according to the prior art.

Description of the Preferred Embodiment

1. Detailed Description of the Drawings

Referring to Fig. 2, the technique for transferring logic signals from a signal transmitting unit 20 to a signal receiving unit 25 according to the present invention is shown. The signals from transmitting unit 20 to receiving unit 25 are transferred by bus 23. At least one signal, bit P, is transferred using the present invention. Signal bit P is applied to an input terminal of inverting amplifier 21 and amplifier 22. While inverting amplifier 21 and amplifier 22 are shown as being included in bus 23, it will be clear these amplifiers can be part of the transmitting unit 20 or can be interposed between transmitting unit 20 and the bus 23. The output terminal of inverting amplifier 21 is

applied to conductor 31, while the output terminal of amplifier 22 is coupled to associated conductor 32, the associated conductors 31 and 32 being part of bus 23. The associated conductors 31 and 32 are applied to the receiving unit 25 and, more particularly, to verification unit 27. Within verification unit 27, conductor 31 is coupled to an inverting input terminal of logic AND gate 271, while conductor 32 is coupled to an input terminal of logic AND gate 27. The output terminal logic AND gate is the transferred logic bit P. The conductor 31 and the conductor 32 are applied to input terminals of logic EXCLUSIVE NOR gate 272. The output terminal of logic EXCLUSIVE NOR gate 272 is coupled to an input terminal of logic OR gate 28. The output terminals of the logic EXCLUSIVE NOR gate associated with each transferred logic bit is applied to logic OR gate 28. The output terminal of logic OR gate 28 provides the EXCEPTION signal.

2. Operation of the Preferred Embodiment

The operation of the present invention can be understood as follows. The associated conductors carry the logic state signal and the complementary logic state signals respectively. In the case of no error being generated, the logic AND gate will reconstitute the transferred logic signal. The logic EXCLUSIVE NOR gate, receiving different logic state signals, generate a logic

O state signal. This logic 0 state signal, when applied to the logic OR gate will not result in the generation of an EXCEPTION signal. When an error occurs in the transfer of a logic signal, one of the logic signals on the associated conductor pair will change logic states. In this situation, the logic signals on both associated conductors are the same. The output signal of the logic AND gate will be a logic 0. Therefore, the error can not write a logic 1 by mistake. In a system in which a logic 0 is considered inactive data or is zero dominant, the system is protected from error. Because the same logic state signals are applied to the terminals of logic EXCLUSIVE NOR gate, the output signal of the logic EXCLUSIVE NOR gate will be a logic 1 signal indicating a signal transmission error. The output signals from the logic EXCLUSIVE NOR gates associated with the transmission of each logic bit signals are applied to the logic OR gate. A logic 1 signal from any of the verification units will result in an EXCEPTION signal, the EXCEPTION signal indicating incorrect signal transmission for one of the group of logic bits.

While the invention has been described with respect to the embodiments set forth above, the invention is not necessarily limited to these embodiments. Accordingly, other embodiment variations, and improvements not described herein, are not necessarily excluded from the

scope of the invention, the scope of the invention being defined by the following claims.